	L #	Hits	Search Text	DBs	Time Stamp
1	L1	2	("5837428").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 14:50
2	L2	6	("4620986" | "4910122" | "5326727" | "5472564" | "5514621" | "5545588").PN.	US-PGPUB; USPAT; USOCR	2005/01/12 14:50
3	L3	13	("5837428").URPN.	USPAT	2005/01/12 15:05
4	L4	118596	pattern$6 near4 (P/R or resist or photoresist or photo-resist or PR)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:06
5	L5	14423	(reduc$6 or etch$6 or pattern$6) near8 (LW or linewidth or "line width")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:07

	L #	Hits	Search Text	DBs	Time Stamp
6	L6	24571	"silicon oxynitride" or SiON or "Si.sub.?O.sub.?N.sub.?"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:08
7	L7	804674	interconnect$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:08
8	L8	168	4 and 5 and 6 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:47
9	L9	520	(second! or another or additional$6) near2 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:48

	L #	Hits	Search Text	DBs	Time Stamp
10	L10	10	8 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:49
11	L11	2	10 and ((@ad<"19970609") or (@rlad<"19970609"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:54
12	L12	448	pattern$6 with (photoresist or resist or P/R) with (SiON or "silicon oxynitride")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:54
13	L13	36155	texas adj instrument	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:54

	L #	Hits	Search Text	DBs	Time Stamp
14	L14	72	12 and ((@ad<"19970609") or (@rlad<"19970609"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:05
15	L15	4	14 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 15:55
16	L16	4	12 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:00
17	L17	0	pattern$6 with (resist or photoresist or P/R) with ("silicon oxynitride" or SiON) with "dummy gate"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:03

	L #	Hits	Search Text	DBs	Time Stamp
18	L18	0	pattern$6 same (resist or photoresist or P/R) same ("silicon oxynitride" or SiON) same "dummy gate"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:03
19	L19	20	pattern$6 same (resist or photoresist or P/R) same ("silicon oxynitride" or SiON) and "dummy gate"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:04
20	L20	0	19 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:05
21	L21	10	19 and ((@ad<"19970609") or (@rlad<"19970609"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:42

	L #	Hits	Search Text	DBs	Time Stamp
22	L22	115	reducing near4 linewidth	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:09
23	L23	1	22 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:12
24	L24	13	linewidth near4 patterned near4 resist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:15
25	L25	1266	pattern$6 near8 (P/R or resist or photoresist) near8 (ARC or antireflective or SiON or "silicon oxynitride")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:17

	L #	Hits	Search Text	DBs	Time Stamp
26	L26	10574	(second! or another or additional$6 or extra) near2 (ARC or antireflective or SiON or "silicon oxynitride")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:18
27	L27	189	25 and 26	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:37
28	L28	3	27 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:41
29	L32	1527	29 or 30 or 31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:42

	L #	Hits	Search Text	DBs	Time Stamp
30	L33	27	32 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:42
31	L34	2	33 and ((@ad<"19970609") or (@rlad<"19970609"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:42
32	L29	243	(438/769).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 16:43
33	L30	1139	(438/585).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 17:54

	L #	Hits	Search Text	DBs	Time Stamp
34	L31	165	(438/952).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 18:40
35	L35	1955	(438/669,672,947).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/12 18:41

US-PAT-NO: 6319857

DOCUMENT-IDENTIFIER: US 6319857 B1

TITLE: Method of fabricating stacked N-O-N ultrathin gate dielectric structures

---------- KWIC ---------

Application Filing Date - AD (1):
19960916

Detailed Description Text - DETX (13):
FIG. 4A shows a preferred embodiment of the present invention. In the gate oxidation step, shown in FIG. 1G, the step is improved by depositing oxynitride 400, typically less than 100 angstroms, in place of oxide. The deposition of the oxynitride 400 facilitates the avoidance of a thin oxide at the location of a particle on the substrate. Rather than growing the oxide on the silicon, the oxynitride layer 400 is deposited over the silicon including any particles which may reside on its surface. Additionally, due to the higher dielectric constant of the oxynitride, the actual thickness of the oxynitride layer 400 can be almost double the conventional oxide layer shown in FIG. 1G while still having an equivalent electrical thickness as the gate oxide shown in FIG. 1G. This thicker layer of oxynitride 400 is typically far easier to work with than the very thin layer of gate oxide.

Current US Cross Reference Classification - CCXR (6):
438/769

US-PAT-NO: 6127262

DOCUMENT-IDENTIFIER: US 6127262 A

TITLE: Method and apparatus for depositing an etch stop layer

---------- KWIC ---------

Application Filing Date - AD (1):
19970507

Brief Summary Text - BSTX (4):
A common step in the fabrication of such devices is the formation of a patterned thin film on a substrate. These films are often formed by etching away portions of a deposited blanket layer. Modern substrate processing systems employ photolithographic techniques to pattern layers. Typically, conventional photolithographic techniques first deposit photoresist or other light-sensitive material over the layer being processed. A photomask (also known simply as a mask) having transparent and opaque regions which embody the desired pattern is then positioned over the photoresist. When the mask is exposed to light, the transparent portions allow for the exposure of the photoresist in those regions, but not in the regions where the mask is opaque. The light causes a chemical reaction in exposed portions of the photoresist. A suitable chemical, chemical vapor or ion bombardment process is then used to selectively attack either the reacted or unreacted portions of the photoresist. With the remaining photoresist pattern acting as a mask, the underlying layer may then undergo further processing. For example, the layer may be doped or etched, or other processing carried out.

Brief Summary Text - BSTX (5):
When patterning such thin films, it is desirable that fluctuations in line

width and other critical dimensions be minimized. Errors in these dimensions can result in variations in device characteristics or open-/short-circuited devices, thereby adversely affecting device yield. Thus, as feature sizes decrease, structures must be fabricated with greater accuracy. As a result, some manufacturers now require that variations in the dimensional accuracy of patterning operations be held to within 5 percent of the dimensions specified by the designer.

Brief Summary Text - BSTX (6):

Modern photolithographic techniques often involve the use of equipment known as steppers, which are used to mask and expose photoresist layers. Steppers often use monochromatic (single-wavelength) light, enabling them to produce the detailed patterns required in the fabrication of fine geometry devices. As a substrate is processed, however, the topology of the substrate's upper surface becomes progressively less planar. This uneven topology can cause reflection and refraction of the monochromatic light, resulting in exposure of some of the photoresist beneath the opaque portions of the mask. As a result, this uneven surface topology can alter the mask pattern transferred to the photoresist layer, thereby altering the desired dimensions of the structures subsequently fabricated.

Brief Summary Text - BSTX (7):

One phenomenon which may result from these reflections is known as standing waves. When a photoresist layer is deposited on a reflective underlying layer and exposed to monochromatic radiation (e.g., deep ultraviolet (UV) light), standing waves may be produced within the photoresist layer. In such a situation, the reflected light interferes with the incident light and causes a periodic variation in light intensity within the photoresist layer in the

vertical direction. Standing-wave effects are usually more pronounced at the deep UV wavelengths used in modern steppers than at longer wavelengths because the surfaces of certain materials (e.g., oxide, nitride and polysilicon) tend to be more reflective at deep UV wavelengths. The existence of standing waves in the photoresist layer during exposure causes roughness in the vertical walls formed when sections of the photoresist layer are removed during patterning, which translates into variations in linewidths, spacing and other critical dimensions.

Brief Summary Text - BSTX (11):

High etch selectivity is desirable in many situations. Examples include processes for creating vias, self-aligned contacts and local interconnect structures. For example, the damascene process sometimes used in creating connections between metal layers can benefit from a layer having high etch selectivity. Damascene is a jewelry fabrication term that has been adopted in the processing of substrates to refer to a metallization process in which interconnect lines are recessed in a planar dielectric layer by patterning troughs in the dielectric layer and then filling the troughs with metal by blanketing the dielectric layer's surface with a layer of metal. Excess metal (i.e., that metal not filling the troughs) is then removed by chemical-mechanical polishing (CMP) or similar method. This is in contrast to traditional processes used to create metal interconnect lines, which usually proceed by forming metal interconnect lines over a dielectric layer and subsequently blanketing the entire structure with one or more layers of dielectric material.

Detailed Description Text - DETX (3):

In a preferred embodiment of the present invention, an antireflective coating (ARC) is deposited to protect layers underlying the ARC from

etchants
used to pattern layers overlying the ARC, and to promote more accurate
patterning of the layer underlying the ARC by reducing the reflection and
refraction of incident light within a **photoresist layer used in the patterning**
operation. According to the method of the present invention, the ARC
preferably includes silicon, nitrogen and oxygen. An ARC having this kind of
composition is referred to herein as a dielectric ARC (DARC), as distinguished
from a more traditional ARC, which is normally organic in composition.
According to the present invention, a DARC may be deposited on a substrate
using a plasma-enhanced chemical vapor deposition (PECVD) technique. To
deposit the DARC, a chemical reaction is promoted between silane (SiH.sub.4)
and nitrous oxide (N.sub.2 O), in the presence of helium (He) and, optionally,
a nitrogen-containing compound (e.g., ammonia (NH.sub.3)), substantially
adjacent to the

Detailed Description Text - DETX (32):
The above reactor description is mainly for illustrative purposes, and other
plasma CVD equipment such as electron cyclotron resonance (ECR) plasma CVD
devices, induction coupled RF high density plasma CVD devices, or the like may
be employed. Additionally, variations of the above-described system, such as
variations in susceptor design, heater design, RF power frequencies, location
of RF power connections and others are possible. For example, the wafer could
be supported and heated by quartz lamps. The film of the present invention,
and method for forming the same is not limited to any specific apparatus or to
any specific plasma excitation method. Moreover, the deposition rate of films
other than silicon nitride and **silicon oxynitride** films may also be controlled
when using the method of the present invention.

Detailed Description Text - DETX (42):

FIG. 3 illustrates the steps performed in a damascene process, and is described with reference to the vertical, cross-sectional views of the structure being fabricated during various points in the fabrication process shown in FIGS. 4A-4E. As noted, a damascene technique uses a planarization step to remove excess metal applied in a blanket over a patterned dielectric layer, leaving metal only in the etched areas of the dielectric. Various structures can be fabricated using a damascene process. For example, metal interconnect layers may be fabricated, as may inter-metal dielectric (IMD) layers, which provide connections between metal interconnect layers known as vias. Such structures increase the density, performance, and reliability of devices thus fabricated. A damascene process also permits the use of otherwise unsuitable metal compositions. Additionally, the resulting surface is more planar than those surfaces created by traditional processes.

Detailed Description Text - DETX (44):

Optionally, first dielectric layer 400 may be patterned, with DARC/ESL 410 acting as an antireflective coating to improve patterning accuracy. First, a photoresist layer is applied and patterned using a mask, thus forming a patterned photoresist layer (not shown) at step 320. The pattern is transferred to DARC/ESL 410 by an etching operation (step 330). This etching operation employs an etchant particularly suited to etching DARC/ESL material (e.g., silicon nitride or silicon oxynitride). At step 340, first dielectric layer 400 is also patterned by an etching operation. The photoresist layer is then removed. Alternatively, the photoresist layer may be removed prior to patterning first dielectric layer 400, and DARC/ESL 410 used as the masking layer during the patterning operation. However, if DARC/ESL 410 is to be used as a mask, DARC/ESL 410 will likely have to be deposited in greater thicknesses

than might otherwise be required.

Detailed Description Text - DETX (45):
Aside from its use as an etch stop layer in later processing steps, DARC/ESL 410 also provides improved accuracy in the patterning of the photoresist layer. By reducing reflection and refraction of the incident radiant energy used to expose the photoresist layer, DARC/ESL 410 reduces the unintentional exposure of photoresist material. DARC/ESL 410 is thus capable of acting as both an antireflective coating and an etch stop layer.

Detailed Description Text - DETX (47):
The deposition of dielectric layer 420 is followed by the application and patterning of photoresist material (using a mask pattern) to form a patterned photoresist layer (not shown) at step 360. The pattern etched into this photoresist layer is then transferred to second dielectric layer 420 by an etching operation (step 370). The result of this operation can be seen in FIG. 4B, in which gaps 430 and 440 serve to exemplify the pattern etched into second dielectric layer 420.

Detailed Description Text - DETX (49):
Optionally, the portions of DARC/ESL 410 exposed by the previous patterning operation (e.g., those portions at the bottom of gaps 430 and 440) may also be removed. Such an operation is performed at step 380. The results of this operation are shown in FIG. 4C. Here, the etching operation employs an etchant particularly suited to etching DARC/ESL material (e.g., silicon nitride or silicon oxynitride), thus leaving first dielectric 400 substantially unaffected.

Claims Text - CLTX (31):
14. The process of claim 12 wherein the second layer is a silicon oxynitride layer.

Related Application Filing Date - RLFD (1):
19960628